WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a nonvolatile memory to store redundant address information or trimming information;

a decoder to decode the redundant address information or the trimming information stored in the nonvolatile memory; and

a switch circuit controlled by the decoder,

wherein the nonvolatile memory includes nonvolatile memory cells each having a first semiconductor area of a first conductivity type formed in a main surface of a semiconductor substrate, and a second semiconductor area of a second conductivity type formed in the main surface of the semiconductor substrate, a source area and a drain area of the second conductivity type formed in the first semiconductor area and a gate electrode formed by interposing an insulating film between the first semiconductor area and the second semiconductor area and a floating gate, and being capable of writing and reading by applying a predetermined voltage to the second semiconductor area and to at least one of the source area and the drain area;

wherein the nonvolatile memory cell is applied with the predetermined voltage to read in accordance with a reset signal, and the redundant address information or the trimming information read from the nonvolatile memory is stored in a register, and

wherein, while the semiconductor integrated circuit device is powered after storing the redundant address information or the trimming information in the register, the redundant address information or the trimming information read from

the nonvolatile memory is held in the register and the nonvolatile memory cell is not applied with the predetermined voltage.

2. The semiconductor integrated circuit device according to claim 1:

wherein the reset signal is generated when the semiconductor integrated circuit device is powered.

3. The semiconductor integrated circuit device according to claim 1:

wherein a logic circuit, the register and a state machine included in the semiconductor integrated circuit are initialized in accordance with the reset signal.

4. The semiconductor integrated circuit device according to claim 1:

wherein data read from the nonvolatile memory is stored in a static register.

5. The semiconductor integrated circuit device according to claim 1, further comprising:

a logic circuit;

a first pad to input a voltage higher than an operation voltage of the logic circuit for a writing operation of the nonvolatile memory; and

a second pad to input or output a signal to or from the logic circuit,

wherein the second pad is connected to an external terminal and the first pad is not connected to an external terminal.